S/N 09/537,274 **PATENT**

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

| | | | |
|---|---|---|---|
| Applicant: | Larry Eugene Mosley | Examiner: Eric W. Thomas | |
| Serial No.: | 09/537,274 | Group Art Unit: 2831 | |
| Filed: | March 29, 2000 | Docket: 884.240US1 | |
| Title: | MULTI-LAYER CHIP CAPACITOR | | |



**AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111**

Commissioner for Patents
Washington, D.C. 20231

The Applicant has reviewed the Office Action mailed on May 23, 2001, including the references cited therewith, and responds within the allotted time. Please amend the above-identified patent application as follows, and consider the appended remarks.

#5/A TE 8/27/01

**IN THE SPECIFICATION**

Please make the paragraph substitutions indicated in the appendix entitled Clean Version of Amended Specification Paragraphs. The specific changes incorporated in the substitute paragraphs are shown in the following marked-up versions of the original paragraphs:

Please amend the paragraph beginning on page 4, line 6, as follows:

Figure 2 illustrates a cross-section of a capacitor of one embodiment of the present invention. The capacitor 200 is fabricated on a substrate 202. Numerous layers of conductor 204 material separated by dielectric 208 are fabricated over the substrate. The conductive layers can be fabricated from any conductive material, such as but not limited to aluminum, copper or a metal alloy. The dielectric layers can be fabricated from any suitable dielectric, such as but not limited to $BaSrTiO_3$ ( referred to herein as BST).

Please amend the paragraph beginning on page 4, line 23, as follows:

The number and size of the vias can be selected to reduce resistance of the capacitor interconnects and allow for C4 mounting to a package. The vias can be connected together in one of three ways. The first interconnect method includes fabricating conducting interconnects on a top surface of the capacitor. These interconnects can be conductive strips that run perpendicular to the conductive strip layers. A second embodiment provides interconnects on a package, or circuit board. The vias, therefore, are each coupled to the interconnects on the package. In a third embodiment, some of the vias are coupled using interconnect lines on the capacitor and some of the vias are coupled using interconnect lines on the circuit board. Independent of how the vias are connected, lands (pads) can be made on the top of the capacitor to form C4 connections to attach to the package substrate.